IEEE Standard Test Access Port and Boundary Scan Register for the ISL5216 (QPDC)

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Introduction:

The test access port (TAP) provided on the ISL5216 is compliant with the IEEE Std 1149.1-1990 TAP. The purpose of this documentation is to describe the specific embodiment of the IEEE Std 1149.1 TAP implemented on the ISL5216 Quad Down Converter. This document does not attempt to describe the IEEE TAP operation in detail.

The IEEE TAP is composed of a TAP controller, test data registers and an instruction register. The TAP provided on the ISL5216 includes five pins. They are:

- TDI - Test Data Input
- TCLK - Test Clock
- TMS - Test Mode Select
- $\overline{\text{TRST}}$ - Active Low Test Reset (Asynchronous)
- TDO - Test Data Output

As recommended in the 1149.1 standard documentation the $\overline{\text{TRST}}$ test pin should be made active soon after power-up to guarantee a known state within the TAP logic on the ISL5216. This avoids potential damage due to signal contention at the circuit's inputs and outputs.

The TAP controller is a state machine which is controlled by the current value of TMS and changes state on the rising edge of TCLK. For every instruction there is a shift register (test data register) connected between the TDI input and the TDO output unless in the SHIFT-IR state. In this case, the instruction register is connected between the same two pins. For most instructions this register is the boundary scan register. All data is loaded serially in the TDI pin through the selected test data register, and serially out the TDO pin. Test data registers must be composed of at least one shift register stage. The shift register stage may have a parallel input as well as the shift register input.

A test data register is updated from its parallel input on the rising edge of TCLK following entry into the CAPTURE-DR state in an instruction which selects that register. Data are shifted through the test data register only during the SHIFT-DR state. A test data register may also contain a parallel output register. This register is loaded from the output of the corresponding shift register cell on the falling edge of TCLK in the UPDATE-DR TAP state.

Both the instruction register and boundary scan register are implemented with a parallel output stage on the ISL5216. Figure 1 displays the basic arrangement of all registers implemented on the ISL5216.

NOTE: The parallel input to the shift registers is not shown in this diagram.

If the test access port provided is not utilized in the circuit where the ISL5216 resides, then the test pins will be pulled as follows:

- TDI - logic 1 (weak pull-up)
- TCLK - logic 0 (weak pull-down)
- TMS - logic 1 (weak pull-up)
- $\overline{\text{TRST}}$ - logic 0 (weak pull-down)
- TDO - will be three-stated by the ISL5216

General Test Data and Instruction Register Configuration

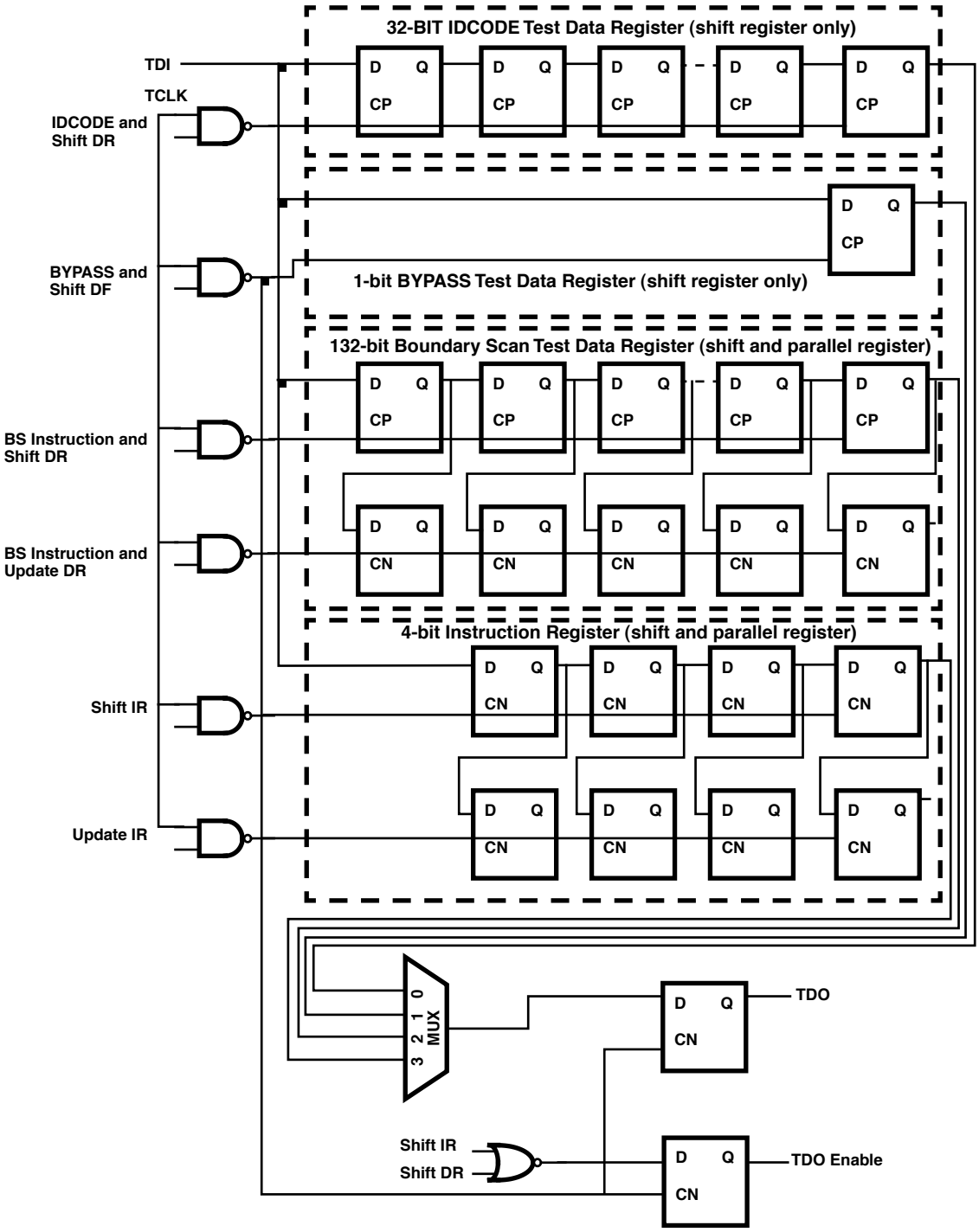


FIGURE 1. GENERAL TEST DATA AND INSTRUCTION REGISTER CONFIGURATION

TABLE 1. BOUNDARY SCAN REGISTER CONFIGURATION

STATE	SAMPLE/PRELOAD						EXTEST						INTEST						OTHER INSTRUCTIONS					
	INPUTS			OUTPUTS			INPUTS			OUTPUTS			INPUTS			OUTPUTS			INPUTS			OUTPUTS		
	SR	PAR	MUX	SR	PAR	MUX	SR	PAR	MUX	SR	PAR	MUX	SR	PAR	MUX	SR	PAR	MUX	SR	PAR	MUX	SR	PAR	MUX
Test-Logic-Reset	RS	RS	PIN	RS	RS	SO	RS	RS	PIN	RS	RS	SO	RS	RS	PIN	RS	RS	SO	RS	RS	PIN	RS	RS	SO
Capture-DR	PIN	RS	PIN	SO	RS	SO	PIN	RS	PAR	RS	RS	PAR	RS	RS	PAR	SO	RS	PAR	RS	RS	PIN	RS	RS	SO
Shift-DR	PSR	RS	PIN	PSR	RS	SO	PSR	RS	PAR	PSR	RS	PAR	PSR	RS	PAR	PSR	RS	PAR	RS	RS	PIN	RS	RS	SO
Update-DR	RS	SR	PIN	RS	SR	SO	RS	RS	PAR	RS	SR	PAR	RS	SR	PAR	RS	SR	PAR	RS	RS	PIN	RS	RS	SO
Other State	RS	RS	PIN	RS	RS	SO	RS	RS	PAR	RS	RS	PAR	RS	RS	PAR	RS	RS	PAR	RS	RS	PIN	RS	RS	SO

SR -shift register stage

RS - retain previous state

PAR - parallel output register

MUX - the multiplexor selecting between the normal pin value or the parallel register value (except the system clock pin).

PSR - previous shift register stage value

PIN - Pad Input Value

SO - System logic output

NOTE: In the test-logic-reset state the instruction is set to IDCODE, therefore only the columns under “All other instructions” is significant

Test Data Registers

There are three test data registers included in the ISL5216 TAP logic. All the required information about each of these registers is given below.

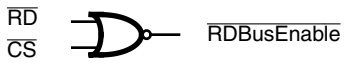
The boundary scan register is 132 bits long. The boundary scan register is composed of a shift register stage and a parallel output register. There are three basic boundary scan cells:

- Boundary Scan In Core
- Boundary Scan Out Core
- Boundary Scan Three-state Cell

The BS_inCore cell is used for all input pins including CLK and $\overline{WR}$, the BS_outTriCore is used for three-state outputs and bidirect pins, and the BS_outCore cell is used for output only pins.The purpose of the boundary scan register is to provide the user the ability to observe the inputs and outputs during various test modes and also the ability to force the circuit”s inputs and outputs to specific states to perform other testing. There is a boundary scan cell for each input and output of the circuit and for each three-state output and bidirect, the cell also contains a shift register and parallel register for that output’s enable signal. The operating modes of the boundary scan register for each instruction in each TAP controller state are shown in Table 1.

The significance of setting each bit of the parallel output register depends upon the instruction currently being executed. If the current instruction selects the parallel output register (PAR) at the boundary scan register cell multiplexer (MUX) then the value currently in the parallel output register will drive that pin of the circuit. Note the exceptions of outputs which can be three-stated. For three-stateable outputs the actual value driven from the circuit pin will be a combination of the values at the output itself and the value from the enable cell. Table 1 gives a thorough account of the operation of the boundary scan register.

In the CAPTURE-DR state of an instruction which selects the boundary scan register the shift register stage is loaded with the value of the respective system pin on the first rising edge of TCLK after entering the CAPTURE_DR state. Note that at three-state outputs both the value at the pin and the value of the enable will be captured.



A capture of any test data register occurs at the rising edge of TCLK. Thus all circuit inputs must be setup to the rising edge of TCLK.

When the boundary scan register is configured to drive the system pins an update of the boundary scan parallel output register will cause the system pins, including CLK and $\overline{WR}$, to change state on the falling edge of TCLK. All system inputs must be setup to the rising edge of the system clock, therefore the first capture must set the data and put a '0' on CLK, and then the next capture must have the same data with a '1' on CLK. The same is true for setting up data for the WRb signal. The first capture must set the data and put a '0' on WRb, and then the next capture must have the same data with a '1' on the $\overline{WR}$ signal. More information about the values to be driven on system inputs is given for those instructions which drive system pins.

In the INTEST instruction the system clock pin, CLK, is controlled via the parallel register. It is important that there be a rising and a falling edge to complete a single step. The data must be shifted in with the CLK signal low, and then the same data must be shifted in again with the CLK signal high.

The same is true for writing data into the part via the $\overline{WR}$ signal.

Table 2 displays all the I/O correspondence and control information required for use of the boundary scan register. The order of the pins is such that location 1 is shifted in from TDI and location 132 is shifted out to TDO during a shift of the boundary scan register. The remaining bits shift as ordered in the table.

TABLE 2. BOUNDARY SCAN REGISTER I/O CORRESPONDENCE

REGISTER LOCATION	SIGNAL PIN NAME	PIN TYPE	PINS CONTROLLED BY ENABLE CELL	VALUE LOADED TO PLACE CONTROLLED PIN IN AN INACTIVE STATE
1	SD2D	OUTPUT	NA	NA
2	SD1D	OUTPUT	NA	NA
3	SYNCD	OUTPUT	NA	NA
4	SD2C	OUTPUT	NA	NA
5	SD1C	OUTPUT	NA	NA
6	SYNCC	OUTPUT	NA	NA
7	SD2B	OUTPUT	NA	NA
8	SD1B	OUTPUT	NA	NA
9	SYNCB	OUTPUT	NA	NA
10	SD2A	OUTPUT	NA	NA
11	SD1A	OUTPUT	NA	NA
12	SYNCA	OUTPUT	NA	NA
13	SERCLK	OUTPUT	NA	NA
14	$\overline{INTRPT}$	OUTPUT	NA	NA
15	SYNCO	OUTPUT	NA	NA
16	SYNCI3	INPUT	NA	NA
17	SYNCI2	INPUT	NA	NA
18	SYNCI1	INPUT	NA	NA
19	SYNCI0	INPUT	NA	NA
20	SYNCI	INPUT	NA	NA
21	D15	INPUT	NA	NA

TABLE 2. BOUNDARY SCAN REGISTER I/O CORRESPONDENCE (Continued)

22	D14	INPUT	NA	NA
23	D13	INPUT	NA	NA
24	D12	INPUT	NA	NA
25	D11	INPUT	NA	NA
26	D10	INPUT	NA	NA
27	D9	INPUT	NA	NA
28	D8	INPUT	NA	NA
29	D7	INPUT	NA	NA
30	D6	INPUT	NA	NA
31	D5	INPUT	NA	NA
32	D4	INPUT	NA	NA
33	D3	INPUT	NA	NA
34	D2	INPUT	NA	NA
35	D1	INPUT	NA	NA
36	D0	INPUT	NA	NA
37	Dm1	INPUT	NA	NA
38	$\overline{\text{ENID}}$	INPUT	NA	NA
39	C15	INPUT	NA	NA
40	C14	INPUT	NA	NA
41	C13	INPUT	NA	NA
42	C12	INPUT	NA	NA
43	C11	INPUT	NA	NA
44	C10	INPUT	NA	NA
45	C9	INPUT	NA	NA
46	C8	INPUT	NA	NA
47	C7	INPUT	NA	NA
48	C6	INPUT	NA	NA
49	C5	INPUT	NA	NA
50	C4	INPUT	NA	NA
51	C3	INPUT	NA	NA
52	C2	INPUT	NA	NA
53	C1	INPUT	NA	NA
54	C0	INPUT	NA	NA
55	Cm1	INPUT	NA	NA
56	$\overline{\text{ENIC}}$	INPUT	NA	NA
57	B15	INPUT	NA	NA
58	B14	INPUT	NA	NA
59	B13	INPUT	NA	NA
60	B12	INPUT	NA	NA
61	B11	INPUT	NA	NA
62	B10	INPUT	NA	NA

TABLE 2. BOUNDARY SCAN REGISTER I/O CORRESPONDENCE (Continued)

63	B9	INPUT	NA	NA
64	B8	INPUT	NA	NA
65	B7	INPUT	NA	NA
66	B6	INPUT	NA	NA
67	B5	INPUT	NA	NA
68	B4	INPUT	NA	NA
69	B3	INPUT	NA	NA
70	B2	INPUT	NA	NA
71	B1	INPUT	NA	NA
72	B0	INPUT	NA	NA
73	Bm1	INPUT	NA	NA
74	$\overline{\text{ENIB}}$	INPUT	NA	NA
75	A15	INPUT	NA	NA
76	A14	INPUT	NA	NA
77	A13	INPUT	NA	NA
78	A12	INPUT	NA	NA
79	A11	INPUT	NA	NA
80	A10	INPUT	NA	NA
81	A9	INPUT	NA	NA
82	A8	INPUT	NA	NA
83	A7	INPUT	NA	NA
84	A6	INPUT	NA	NA
85	A5	INPUT	NA	NA
86	A4	INPUT	NA	NA
87	A3	INPUT	NA	NA
88	A2	INPUT	NA	NA
89	A1	INPUT	NA	NA
90	A0	INPUT	NA	NA
91	Am1	INPUT	NA	NA
92	$\overline{\text{ENIA}}$	INPUT	NA	NA
93	P15	BIDIRECTIONAL	NA	NA
94	NA	OUTPUT ENABLE	P15	LOGIC 1
95	P14	BIDIRECTIONAL	NA	NA
96	NA	OUTPUT ENABLE	P15	LOGIC 1
97	P13	BIDIRECTIONAL	NA	NA
98	NA	OUTPUT ENABLE	P15	LOGIC 1
99	P12	BIDIRECTIONAL	NA	NA
100	NA	OUTPUT ENABLE	P15	LOGIC 1
101	P11	BIDIRECTIONAL	NA	NA
102	NA	OUTPUT ENABLE	P15	LOGIC 1
103	P10	BIDIRECTIONAL	NA	NA

TABLE 2. BOUNDARY SCAN REGISTER I/O CORRESPONDENCE (Continued)

104	NA	OUTPUT ENABLE	P15	LOGIC 1
105	P9	BIDIRECTIONAL	NA	NA
106	NA	OUTPUT ENABLE	P15	LOGIC 1
107	P8	BIDIRECTIONAL	NA	NA
108	NA	OUTPUT ENABLE	P15	LOGIC 1
109	P7	BIDIRECTIONAL	NA	NA
110	NA	OUTPUT ENABLE	P15	LOGIC 1
111	P6	BIDIRECTIONAL	NA	NA
112	NA	OUTPUT ENABLE	P15	LOGIC 1
113	P5	BIDIRECTIONAL	NA	NA
114	NA	OUTPUT ENABLE	P15	LOGIC 1
115	P4	BIDIRECTIONAL	NA	NA
116	NA	OUTPUT ENABLE	P15	LOGIC 1
117	P3	BIDIRECTIONAL	NA	NA
118	NA	OUTPUT ENABLE	P15	LOGIC 1
119	P2	BIDIRECTIONAL	NA	NA
120	NA	OUTPUT ENABLE	P15	LOGIC 1
121	P1	BIDIRECTIONAL	NA	NA
122	NA	OUTPUT ENABLE	P15	LOGIC 1
123	P0	BIDIRECTIONAL	NA	NA
124	NA	OUTPUT ENABLE	P15	LOGIC 1
125	$\overline{RD}$	INPUT	NA	NA
126	$\overline{WR}$	INPUT	NA	NA
127	ADD1	INPUT	NA	NA
128	ADD0	INPUT	NA	NA
129	$\overline{CE}$	INPUT	NA	NA
130	DSTROBE	INPUT	NA	NA
131	$\overline{RESET}$	INPUT	NA	NA
132	CLK	INPUT	NA	NA

IDCODE Register

The IDCODE register is a 32-bit shift register. In the CAPTURE-DR state of the IDCODE instruction the IDCODE register is loaded with a unique identification code. This code is a compressed form of the JEDEC Publication 106-A. For details see the IEEE TAP standard document. The value loaded into the IDCODE register is:

- Version: 0101
- Part Number: 0001010001100000
- Manufacturer Identity: 00000001011
- LSB: 1

In the IDCODE instruction and SHIFT-DR state the IDCODE register is shifted out of the TDO pin least significant bit first. In any other state of any instruction this register retains its previous state. This code allows the user to identify all chips which have implemented the IDCODE instruction. There is no supplementary identification code for the ISL5216.

TABLE 3. IDCODE TEST DATA REGISTER OPERATION

	INSTRUCTIONS	
STATE	IDCODE	OTHERS
CAPTURE-DR	Loaded with IDCODE value (51460017)h	Retains Previous State
SHIFT-DR	Shifted out TDO pin	Retains Previous State
OTHER	Retains Previous State	Retains Previous State

BYPASS Register

The bypass register is a 1-bit shift register. In the CAPTURE-DR state of the BYPASS instruction or any of the undefined instructions (undefined instructions are required to operate exactly like the BYPASS instruction) a value of 0 is captured into this register. In the SHIFT-DR state of the same instructions the value is shifted out the TDO pin. This register is used to create the shortest possible path between the TDI and TDO pins. The significance of the logic 0 loaded in the CAPTURE-DR state is to identify it as a BYPASS register rather than an IDCODE register (an IDCODE register has a logic '1' always as its least significant bit).

TABLE 4. BYPASS TEST DATA REGISTER

STATE	STATE	
	BYPASS OR UNDEFINED	OTHER
CAPTURE-DR	LOGIC 0	RETAINS PREVIOUS STATE
SHIFT-DR	SHIFTED OUT TDO PIN	RETAINS PREVIOUS STATE
OTHER	RETAINS PREVIOUS STATE	RETAINS PREVIOUS STATE

Instruction Register

The instruction register is four bits long. The instructions do not have a parity bit. In the CAPTURE-IR controller state the value loaded into the instruction shift register is "0001". The two most significant zeros loaded into the instruction shift register during the CAPTURE-IR controller state have no design-specific significance.

Public Instructions

All of the public instructions supported by the ISL5216 are listed with their binary code, test data register selected between TDI and TDO and the significance of that register in Table 5. For the configuration of the boundary scan test data register in any of these instructions see Table 1. Each of the instructions will be described in more detail below.

TABLE 5. IEEE TAP INSTRUCTIONS

INSTRUCTION BINARY CODE	NAME	TEST DATA REGISTER SELECTED	SIGNIFICANCE OF DATA LOADED INTO TDR IN THE CAPTURE-DR STATE
0000	EXTEST	BOUNDARY SCAN (132 BITS)	CAPTURES THE INPUTS ONLY
0001	IDCODE	IDCODE (32 BITS)	LOADS THE ISL5216 IDCODE
0010	SAMPLE/PRELOAD	BOUNDARY SCAN (132 BITS)	CAPTURES BOTH THE INPUTS AND OUTPUT FROM CORE
0011	INTEST	BYPASS REGISTER (1 BIT)	CAPTURES ONLY THE OUTPUT FROM CORE
0100	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
0101	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
0110	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
0111	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1000	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1001	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1010	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1011	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1100	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1101	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1110	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)
1111	UNDEFINED	BYPASS REGISTER (1 BIT)	LOADS 0 (OPERATES AS BYPASS)

EXTEST

This instruction has a binary code of 0000. This instructions configures only the boundary scan register in a test mode of operation. The boundary scan register is the serial test data register enabled to shift data in this instruction. The operation of the boundary scan register during this instruction is defined in Table 1.

NOTE: Only the outputs are updated. The input cell values remain the same throughout the EXTEST instruction.

The EXTEST instruction forces the circuit outputs with data from the boundary scan parallel output register on the falling edge of TCLK after the UPDATE-IR instruction initially loads the EXTEST instruction. This part has also been configured to drive the inputs during the EXTEST instruction, which is a valid option. Thus it is recommended that the parallel output stage of the boundary scan register be loaded with known data prior to entering the EXTEST instruction. This would most likely be done using a SAMPLE/PRELOAD instruction just prior to the EXTEST instruction.

The recommended values to load into the inputs cells of the boundary scan register are shown in Table 1. For the EXTEST instruction these values are recommended but *not required*. The part will not be damaged by random data driven on the inputs however the state of the circuit may be forced into an unknown configuration. The values loaded at output pins is determined by the user.

The EXTEST instruction is intended to test the connection between elements on a board. The user loads the boundary scan register outputs with data which are then driven through each circuits output pins. The user would then enter the CAPTURE-DR controller state where the inputs of each circuit are captured. The output values are not captured in this instruction. The boundary scan register can then be shifted out and the shifted data compared to expected values thus checking the connectivity of the board in question.

NOTE: Bi-directional microprocessor interface, pins P(0–15) are only available as outputs in EXTEST mode. However, they are readable in SAMPLE/PRELOAD mode.

IDCODE

The IDCODE instruction has binary value 0001. Only the IDCODE register is placed in a test mode of operation by this instruction. The IDCODE instruction selects the IDCODE register as the serial data path between TDI and TDO. In addition to normal loading of this instruction (via a SHIFT-IR then UPDATE-IR of 0001) this instruction is entered automatically on the falling edge of TCLK after entering the TEST-LOGIC-RESET state or asynchronously upon the activation of $\overline{\text{TRST}}$. The unique identification code entered into the IDCODE register in the CAPTURE-DR state is described in Table 3. This instruction is intended to allow the user to identify all the components on a board. Each component has a unique identification code which is stored in the IDCODE register on any part which implements this instruction. Any part which does not implement the IDCODE instruction must implement the BYPASS instruction for the same binary code as the IDCODE instruction. This is the reason that the least significant bit of the IDCODE is a '1' while the BYPASS register is loaded with a '0'. When all components are running the IDCODE instruction and data is being shifted out of the components following a CAPTURE-DR a '1' initially received indicates that the next 31 bits will be an identification code whereas a 0 indicates no identification code is forthcoming.

SAMPLE/PRELOAD

The binary code of the SAMPLE/PRELOAD instruction is 0010. Only the boundary scan test data register is placed in a test mode of operation during this instruction. The boundary scan test data register is the serial test data register path enabled to shift data between TDI and TDO in this instruction. In the CAPTURE-DR state of this instruction ALL system pins and three-state enable signals are captured into the boundary scan shift register. These values can then be shifted out the TDO pin. In the UPDATE-DR state ALL of the boundary scan register is loaded from the boundary scan shift register. This instruction does not affect the normal operation of the circuit. This instruction can be used to initialize the state of the boundary scan register for different instructions which when entered use values stored in the boundary scan register to immediately drive the state of system pins such as in the INTEST, and EXTEST instructions.

INTEST

The INTEST instruction has binary code 0011. Only the boundary scan test data register is placed in a test mode of operation during this instruction. The boundary scan test data register is the serial test data register path enabled to shift data between TDI and TDO in this instruction. In the CAPTURE-DR state of this instruction only the state of output pins and the three-state enable signals are captured. The input cells of the boundary scan register retain their previous state. In the UPDATE-DR state both input and output cells are updated from their respective shifter register stage. The state of all inputs and outputs of the system, including CLK and WRb are driven with the value stored in the parallel output register of the boundary scan register for the duration of the INTEST instruction. The I/Os are driven immediately following the falling edge of TCLK which loaded the INTEST instruction (in the UPDATE-IR controller state). It may be necessary to use an instruction such as SAMPLE/PRELOAD to configure the boundary scan register prior to executing this instruction.

This instruction is included so that the component may be tested in a single step mode. Typically this instruction would work as follows:

1. Stimulus data for inputs and configuration data for outputs is shifted into the boundary scan register in the SHIFT-DR state, data shifted in for CLK should be “0’;
2. This data is loaded into the boundary scan parallel register in the UPDATE-DR state. This data now drives the inputs and outputs of the part.
3. Go back to the SHIFT-DR state, and shift in the same data again, but this time take the CLK signal to a ‘1’.
4. This data is loaded into the boundary scan parallel register in the UPDATE-DR state. This now drives the inputs and outputs of the part. It guarantees the setup and hold to the core for the internal CLK signal. (The same would be true for WRb if the user is writing control data into the part.)
5. After cycling the clock the test logic is taken into the CAPTURE-DR state where the result of the single clock step is now captured into the shift register stage of the boundary scan register.
6. This data is shifted out the TDO pin in the SHIFT-DR state and compared against known data or analyzed by the user. At the same time the next single step test vector can be shifted in TDI. Repeat step 2. This operation can occur for as many cycles as the user wishes.

NOTE: The system clock pin, CLK, and write pin, WRb, is controlled by the boundary scan register. The user must therefore load each phase of this clock and WRb when attempting to cycle the part or to load control words in the INTEST instruction.

BYPASS

The BYPASS instructions have codes 1100 to 1111. Any undefined instruction must operate as the BYPASS instruction, hence the multiple binary codes. Only the 1-bit BYPASS register is placed in a test mode of operation during this instruction. The BYPASS register is connected between TDI and TDO for shifting operations. There is no requirement to load any data prior to running this instruction.

This instruction is intended to create a minimum length serial path between TDI and TDO for the circuit. In the CAPTURE-DR controller state a 0 is loaded into the BYPASS register. This value distinguishes a BYPASS register from IDCODE registers.

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